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Seventh Semester B.E. Degree Examination, June/July 2025 Advanced Computer Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. With a neat diagram, explain the elements of a modern computer system. (07 Marks)
 b. Consider the execution of an object code with 20,00,000 instructions as a 400 MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based the result of a program trace experiment.

Instruction type	CPI	Instruction Mix
Arithmetic and logic	1	60%
Load / Store with Cache hit	2	18%
Branch	4	12%
Memory Reference with cache miss	8	10%

- (i) Calculate the average CPI when program is executed as a uniprocessor system with the above trace results.
 (ii) Calculate the corresponding MIPS rate based on the CPI obtained.
 (iii) Find the execution time for this program. (06 Marks)
- c. Compare Amdahl's law and Gustafson's speedup performance laws with neat graphs and sketches by taking the parameters workload, no. of processors and execution time. (07 Marks)

OR

- 2 a. List the performance factors and system attributes. Explain how performance factors are influenced by system attributes. (07 Marks)
 b. Determine the parallelism in the following code using Bernstein's conditions. (Assume non pipeline)
 $P_1 : C = D * E ; P_2 : M = G + C ; P_3 : A = B + C ; P_4 : C = L + M ; P_5 : G/E$ (06 Marks)
 c. With a diagram, illustrate the operation of tagged token data flow computer. (07 Marks)

Module-2

- 3 a. Distinguish between RISC and CISC processor architectures, with block diagrams. (07 Marks)
 b. Describe inclusions, coherence and locality properties with respect to the information stored in a memory hierarchy. (09 Marks)
 c. Illustrate any two page replacement policies with the help of an example. (04 Marks)

OR

- 4 a. With a neat sketch, explain the functionality of VLIW architecture. How does it differ from superscalar processor? (10 Marks)
- b. With a neat diagram, explain the hierarchical memory from low level to high level in detail. (06 Marks)
- c. Differentiate scalar and superscalar processor. (04 Marks)

Module-3

- 5 a. Illustrate synchronous and asynchronous bus timing protocols with suitable diagrams. (07 Marks)
- b. Consider the following reservation table of a non-linear pipe line shown below :
- | | | | | | | | | |
|----------------|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| S ₁ | X | | | | | X | | X |
| S ₂ | | X | | X | | | | |
| S ₃ | | | X | | X | | X | |
- (i) What are forbidden latencies?
- (ii) What is the initial collision vector?
- (iii) Draw the state transition diagram.
- (iv) List all simple and freddy cycles.
- (v) Determine MAL. (06 Marks)
- c. Explain direct mapping cache organization. (07 Marks)

OR

- 6 a. Illustrate central and distributed bus arbitration techniques with suitable diagrams. (08 Marks)
- b. Discuss different cache performance issues in detail. (07 Marks)
- c. Explain the features of non linear pipeline processor with feed forward and feedback connections. (05 Marks)

Module-4

- 7 a. Explain cross bar networks and cross point switch design in multiprocessor system. (08 Marks)
- b. Distinguish between store-and-forward routing and wormhole routing schemes. (08 Marks)
- c. Briefly explain "Pre-fetching Technique" for latency hiding and its benefits". (04 Marks)

OR

- 8 a. Define cache coherence problem. Describe cache coherence problems in data sharing and process migration. (08 Marks)
- b. With a neat diagram, explain S-access and C/S-access organization for m-way interleaved memory. (08 Marks)
- c. Discuss various context-switching policies. (04 Marks)

Module-5

- 9 a. With a neat sketch, explain the compilation phases in parallel code generation. (08 Marks)
- b. Illustrate the concept "Operator Forwarding" with suitable examples. (06 Marks)
- c. With the help of a block diagram, discuss the role of reservation stations used in Tomasulo's Algorithm. (06 Marks)

OR

- 10 a. Explain the concurrent OOP and an actor model in object oriented model. (07 Marks)
- b. Describe in brief the use of "Re-order buffer and register Renaming" to address the various types of dependences in the program. (08 Marks)
- c. Discuss any two dependence testing algorithms in detail. (05 Marks)