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14ELD14

First Semester M.Tech. Degree Examination, Dec.2014/Jan.2015
Digital Circuits and Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Find the function $f(x_1, x_2, x_3, x_4)$ realized by the threshold network shown in Fig.Q.1(a). Show the map. **(06 Marks)**

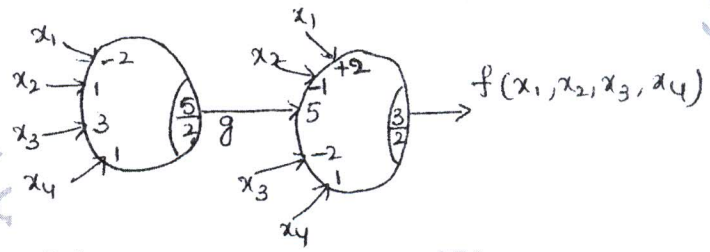

Fig.Q.1(a)

b. Prove that every threshold function is Unate. **(04 Marks)**

c. Given the switching function $f(x_1, x_2, x_3, x_4) = \Sigma(2, 3, 6, 7, 10, 12, 14, 15)$. Find a minimal threshold logic realization. **(10 Marks)**

2 a. In the network shown in Fig.Q.2(a) wires m, n, p and q may become either s – a – 0 or s – a – 1, while the remaining wires are considered "safe".

i) Construct a fault table.

ii) Find a minimal cover of the table and use it to determine a minimal fault detection experiment. **(12 Marks)**

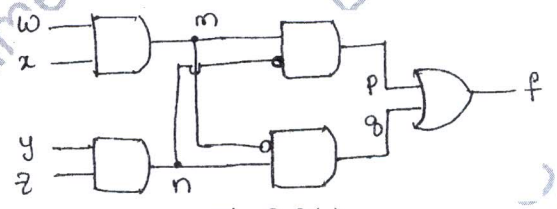

Fig.Q.2(a)

b. Find a preset set of tests to locate all single faults and show the corresponding fault dictionary for the fault table shown below in Fig.Q.2(b) where Z is fault free O/P. **(08 Marks)**

Fault / Tests	F_1	F_2	F_3	F_4	F_5	F_6	Z
T_1					1	1	0
T_2	1		1		1		1
T_3				1	1		0
T_4		1	1				1
T_5	1					1	1
T_6	1		1			1	1

Fig.Q.2(b)

3 a. Use map method to find a minimal set of tests for multiple faults of the function. $f(w, x, y, z) = wz' + xy' + w'x + wx'y$. **(10 Marks)**

b. For the circuit shown in Fig.Q.3(b) find tests to detect the faults h s-a-o and k s-a-1 using Boolean difference method? **(06 Marks)**

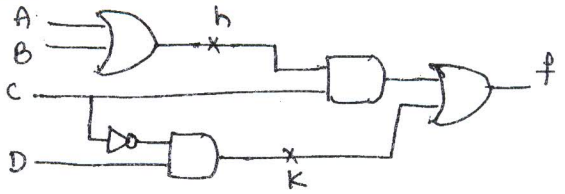

Fig.Q.3(b)

c. Show the Quadded logic realization for the circuit shown in Fig.Q.3(c). **(04 Marks)**

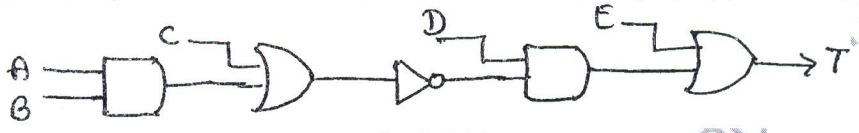

Fig.Q.3(c)

4 a. For the machine shown in Fig.Q4(a). Find the equivalence partition and a corresponding reduced machine in standard form. **(10 Marks)**

PS	NS, Z	
	X = 0	X = 1
A	E, 0	C, 0
B	C, 0	A, 0
C	B, 0	G, 0
D	G, 0	A, 0
E	F, 1	B, 0
F	E, 0	D, 0
G	D, 0	G, 0

Fig.Q.4(a)

PS	NS, Z			
	I_1	I_2	I_3	I_4
A	-	C, 1	E, 1	B, 1
B	E, 0	-	-	-
C	F, 0	F, 1	-	-
D	-	-	B, 1	-
E	-	F, 0	A, 0	D, 1
F	C, 0	-	B, 0	C, 1

Fig.Q.4(b)

b. Draw the merger graph and its minimal form for the machine in Fig.Q.4(b). **(10 Marks)**

5 a. For the machine given in Table 5(a), determine the π - lattice. **(06 Marks)**

b. Define: i) Input-consistent ii) Output-consistent with respect to machines. **(04 Marks)**

c. For the machine shown in Table 5(c), obtain a serial decomposition.

Table 5(a)

PS	NS	
	x = 0	x = 1
A	E	B
B	E	A
C	D	A
D	C	F
E	F	C
F	E	C

Table 5(c)

PS	NS		
	x = 0	x = 1	Z
A	G	D	1
B	H	C	0
C	F	G	1
D	E	G	0
E	C	B	1
F	C	A	0
G	A	E	1
H	B	F	0

$\pi_0 = \pi(0)$

$\pi_a = \{\overline{A,B,G,H}; \overline{C,D,E,F}\}$

$\pi_b = \{\overline{A,B}; \overline{C,D}; \overline{E,F}; \overline{G,H}\}$

$\lambda_o = \{\overline{A,C,E,G}; \overline{B,D,F,H}\}$. **(10 Marks)**

6 The machine shown in table 6 has the following output consistent and input consistent partitions: $\lambda_o = \{\overline{A,E,F}; \overline{B,D}; \overline{C,G}\}$, $\lambda_i = \{\overline{A,E,F}; \overline{B,C,D,G}\}$.

i) List all other closed partitions.

ii) Use state splitting to decompose the machine into components which operate in parallel. **(20 Marks)**

Table 6

PS	NS		Output	
	x = 0	x = 1	x = 0	x = 1
A	B	C	0	0
B	A	F	1	1
C	F	E	1	0
D	F	E	1	1
E	G	D	0	0
F	D	B	0	0
G	E	F	1	0

7 a. Explain the Homing experiments with examples. **(10 Marks)**

b. Explain the adaptive distinguishing experiment by considering the machine shown in Table 7(b). **(10 Marks)**

Table 7(b)

PS	NS, Z	
	x = 0	x = 1
A	C, 0	A, 1
B	D, 0	C, 1
C	B, 1	D, 1
D	C, 1	A, 0

8 a. Explain the general procedure-for fault detection experiment for the machine that has a distinguishable sequence with repeated symbols. Apply the same to the machine in Table 8(a). **(10 Marks)**

PS	NS, ZZ_1	
	x = 0	x = 1
A	B, 01	B, 00
B	A, 00	B, 00
C	D, 10	A, 01
D	D, 11	C, 01

Table 8(a)

b. Design a diagnosable machine for the machine in Table 8(b), write testing table and testing graph for that machine. **(10 Marks)**

PS	NS, Z	
	x = 0	x = 1
A	B, 0	D, 0
B	A, 0	B, 0
C	D, 1	A, 0
D	D, 1	C, 0

Table 8(b)

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