EC 1st year
M.Tech

USN | | | | | | | | | | |

14ELD14

First Semester M.Tech. Degree Examination, June/July 2015
Digital Circuits and Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

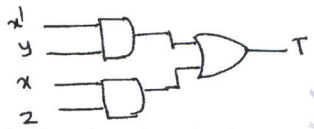
1 a. Discuss the capabilities and limitations of threshold logic. **(06 Marks)**

b. Derive the elementary properties of threshold element. **(06 Marks)**

c. Find a minimal threshold logic realization for the given switching function: $f(r_1, r_2, r_3, r_4) = \sum(2, 3, 6, 7, 10, 12, 14, 15)$. **(08 Marks)**

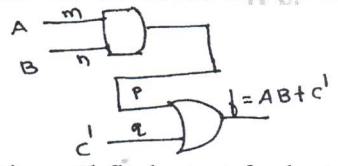
2 a. Analyze the circuit shown in Fig.Q.2(a) for static hazards, redesign the circuit so that it becomes hazard free. **(06 Marks)**

Fig.Q.2(a)



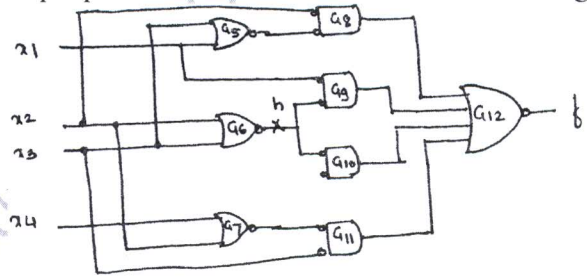
b. Explain and construct the fault table for the circuit shown in Fig.Q.2(b) **(08 Marks)**

Fig.Q.2(b)



c. Apply Boolean difference properties and find a test for h at s-a-o. Fig.Q.2(c). **(06 Marks)**

Fig.Q.2(c)



3 a. Use systematic generation of minimal fault detection experiments and find a-test and also b-tests. For the given function: $f = x_4x_3 + x_4'x_3'x_2 + x_5x_4x_1 + x_5'x_4x_2'x_1'$. **(12 Marks)**

b. Explain the significance of quadded logic. Brief out the operation of NOR-NOR quadded networks. **(08 Marks)**

4 a. Define finite state machines and discuss the limitation on capability of finite state machine with an example of serial binary multiplier. **(06 Marks)**

b. Find the equivalence partition and corresponding reduced equivalent machine for given machine M_1. **(08 Marks)**

M1

PS	NS, Z	
	x = 0	x = 1
A	E, 0	D, 1
B	F, 0	D, 0
C	E, 0	B, 1
D	F, 0	B, 0
E	C, 0	F, 1
F	B, 0	C, 0

c. Draw the merger graph and compatibility graph to bring to its minimal form for machine M_2. **(06 Marks)**

M_2

PS	NS, Z			
	I_1	I_2	I_3	I_4
A	-	-	E, 1	-
B	C, 0	A, 1	B, 0	-
C	C, 0	D, 1	-	A, 0
D	-	E, 1	B, -	-
E	B, 0	-	C, -	B, 0

5 a. Obtain the π-lattice closed partitions of the machine. **(10 Marks)**

M_3

PS	NS		Z
	x = 0	x = 1	
A	H	B	0
B	F	A	0
C	G	D	0
D	E	C	1
E	A	C	0
F	C	D	0
G	B	A	0
H	D	B	0

b. Express explicitly in each case the dependency of the output and the state variables for machine M_4. **(10 Marks)**

M_4

PS	NS, Z	
	x = 0	x = 1
A	A, 0	D, 1
B	A, 0	C, 0
C	C, 0	B, 0
D	C, 0	A, 1

Assignment α	Assignment β
A – 00	A – 00
B – 01	B – 01
C – 11	C – 10
D – 10	D – 11

6 a. Find the closed partitions, draw implication graph and closed cover for the machine M_5. **(10 Marks)**

M_5

PS	NS, Z	
	x = 0	x = 1
A	B, 0	C, 0
B	A, 1	F, 1
C	F, 1	E, 0
D	F, 1	E, 1
E	G, 0	D, 0
F	D, 0	B, 0
G	E, 1	F, 0

b. Define the following:
i) Closed partition ; ii) Lattice ; iii) Implication graph ; iv) Serially decomposable machines ; v) Partition pair. **(10 Marks)**

7 a. Explain the input independence and autonomous clock with a common example. Realize the machine taken as example. **(06 Marks)**

b. For the machine M_6 given find closed partitions specify all the possible ways of decomposing the machine: **(10 Marks)**

M_6

PS	NS, Z		Z
	x = 0	x = 1	
A	G	D	1
B	H	C	0
C	F	G	1
D	E	G	0
E	C	B	1
F	C	A	0
G	A	E	1
H	B	F	0

c. Write a short note on decomposing the composite machines. **(04 Marks)**

8 a. Design a successor tree for machine M_7. **(06 Marks)**

M_7

PS	NS, Z	
	x = 0	x = 1
A	C, 0	D, 1
B	C, 0	A, 1
C	A, 1	B, 0
D	B, 0	C, 1

b. Find the shortest homing sequence for machine M_8. **(06 Marks)**

M_8

PS	NS, Z	
	x = 0	x = 1
A	B, 0	D, 0
B	C, 1	D, 0
C	B, 0	A, 1
D	D, 1	C, 1

c. What are definitely diagnosable machines? Check whether or not distinguishable sequence exists for the machine M_9. Derive the testing graph for the same. **(08 Marks)**

M_9

PS	NS, ZZ_1	
	x = 0	x = 1
A	B, 01	D, 00
B	A, 00	B, 00
C	D, 10	A, 01
D	D, 11	C, 01

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