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10EC46

Fourth Semester B.E. Degree Examination, Dec.2013/Jan.2014
Linear ICs and Applications

Time: 3 hrs. Max. Marks:100

Note: *1. Answer FIVE full questions, selecting at least TWO questions from each part.*
2. Missing data, if any, may be assumed.

PART – A

1 a. Explain common mode voltage, common mode voltage gain and common mode rejection ratio for operational amplifiers. Show that $V_{\theta(cm)} = \frac{V_{i(cm)}}{CMRR} * A_v$ **(10 Marks)**

b. Sketch an op-amp difference amplifier circuit. Derive an equation for the output voltage and explain the operation. **(05 Marks)**

c. A non-inverting amplifier is to amplify a 100 mV signal to a level of 3V, using 741 op-amp design a suitable circuit. [Consider $I_{B(max)}$ = 500 nA, R_s= 1 kΩ]. **(05 Marks)**

2 a. Sketch and explain the operation of a capacitor coupled inverting amplifier circuit using a single polarity supply with necessary design steps. **(08 Marks)**

b. Sketch the circuit of a high input impedance capacitor coupled non-inverting amplifier. Briefly explain its operation and show that the input impedance is very high compared to capacitor coupler non-inverting amplifier. **(06 Marks)**

c. Design high input impedance capacitor coupled voltage follower using an op-amp having lower cut-off frequency of 50 Hz and maximum input bias current of 500 nA. The load resistance is 3.9 kΩ. If the open loop gain is 2×10^5. Find the value of input impedance. [Consider $M_{(min)}$ = 50,000]. **(06 Marks)**

3 a. Explain phase-lag and phase-lead compensation methods. **(08 Marks)**

b. List the precautions to be observed for op-amp circuit stability. **(08 Marks)**

c. Determine the upper cut-off frequency and maximum distortion free output amplitude of a voltage follower when a 741 op-amp is used. **(04 Marks)**

4 a. Draw the circuit of instrumentation amplifier, discuss the characteristics of the circuit and show how voltage gain can be varied. Also show the method of nulling common mode outputs and how dc output voltage can be level shifted. **(12 Marks)**

b. A voltage source is to be designed to provide constant output voltage of approximately 6V. The load resistance has a minimum value of 150 Ω and the available supply voltage is ±12V. Design a suitable circuit using IC 741 and a zener diode with a V_Z of 6.3 V. Sketch the circuit with designed components. [Consider I_z = 20 mA]. **(08 Marks)**

PART – B

5 a. Draw and explain an op-amp sample and hold circuit with signal control and output waveforms. **(08 Marks)**

b. Explain op-amp square wave/ triangular wave generator with circuit diagram, waveform and expressions. **(08 Marks)**

c. Using a BIFET op-amp with a supply of ±12V, design a wein bridge oscillator to have an output frequency of 15 kHz. **(04 Marks)**

6 a. With a neat circuit diagram, waveform and expressions, explain the capacitor coupled non-inverting cross detector. **(08 Marks)**

b. With a neat circuit diagram, explain how diodes may be used to select the trigger points of an inverting Schmitt trigger circuit. **(06 Marks)**

c. Design a second order low pass filter circuit to have a cutoff frequency of 1 kHz (for 741 frequency extends upto 800 kHz with $A_v = 1$). **(06 Marks)**

7 a. With a neat functional diagram, explain the operation of low voltage regulator using IC 723. **(08 Marks)**

b. List out the limitations of linear voltage regulators. **(06 Marks)**

c. Define the following performance parameters of a voltage regulator:
(i) Line regulation (ii) Load regulation (iii) Ripple regulation. **(06 Marks)**

8 a. Explain the working of monostable multivibrator using 555 timer with a neat functional diagram and waveforms. Derive the equation for its pulse width. **(08 Marks)**

b. Draw the block diagram representation of PLL and explain. **(06 Marks)**

c. An 8-bit ADC outputs all 1's when $V_i = 2.55$ V. Find its (i) resolution in mV/LSB and ii) Digital output when $V_i = 1.28$ V. **(06 Marks)**

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