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10ES33

Third Semester B.E. Degree Examination, Dec.2014/Jan.2015
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Design a combinational circuit which takes two, 2 – bit binary numbers as its input and generates an output equal to 1, when the sum of the two numbers is odd. **(06 Marks)**

b. Convert the given Boolean function into :

i) $R = f(a,b,c) = (\bar{a} + b)(b + \bar{c})$ minterm canonical form

ii) $P = f(x,y,z) = x + \overline{xz}(y + \bar{z})$ maxterm canonical form. **(06 Marks)**

c. Distinguish prime implicant and essential prime implicant. Determine PI and EPI for the given function N = f(a, b, c, d) = π(0, 1, 4, 5, 8, 9, 11) + d(2, 10) . Simplify the given function and implement using logic gates. **(08 Marks)**

2 a. Simplify the given Boolean function using Quine – Mccluskey method :
Y = f(a, b, c, d) = Σ(0, 1, 2, 6, 7, 9, 10, 12) + d(3, 5). Verify the result using k-map. **(10 Marks)**

b. Find the minimal sum and minimal product for the given Boolean function, using MEV technique : Solve by using 3-variable map and 2 – variable map y = f(a, b, c, d) = Σ(2, 3, 4, 5, 13, 15) + d(8, 9, 10, 11). **(10 Marks)**

3 a. Distinguish between a decoder and an encoder. Implement full adder using IC 74138. **(08 Marks)**

b. Implement 3 – bit binary to gray code conversion by using IC 74139. **(06 Marks)**

c. Design a priority encoder for a system with a 3 inputs, the middle bit with highest priority encoding to 10, the MSB with next priority encoding to 11, while the LSB with least priority encoding to 01. **(06 Marks)**

4 a. Realize the following Boolean function : P = f(w, x, y, z) = Σ(0, 1, 5, 6, 7, 10, 15) using :
i) 16 to 1 MUX ii) 8 : 1 MUX iii) 4 : 1 MUX. **(10 Marks)**

b. With a neat logic diagram, explain carry look ahead adder. **(10 Marks)**

PART – B

5 a. Explain the working of a master –slave SR flip-flop with the help of a logic diagram, function table, logic symbol and timing diagram. **(10 Marks)**

b. With a neat logic diagram, explain the working of positive edge triggered D flip-flop. **(10 Marks)**

6 a. Obtain the characteristic equation for D and T flip-flop. **(06 Marks)**

b. With a neat logic diagram, explain the operation of 4-bit SISO unidirectional shift register. **(06 Marks)**

c. Explain the working of four-bit binary ripple up counter, configured using positive edge triggered flip-flop. Also draw the timing diagram. **(08 Marks)**

7 a. Design synchronous mod-6 counter using D flip-flop to generate the sequence 0, 2, 3, 6, 5, 1, 0 …….. . **(10 Marks)**

b. Compare Mealy and Moore sequential circuit models. **(04 Marks)**

c. Analyze the sequential circuit shown in Fig. Q7(c). **(06 Marks)**

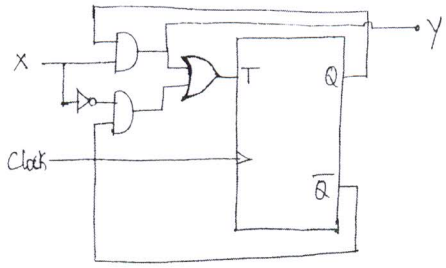

Fig. Q7(c)

Write input and output equations, transition table, state table and state diagram.

8 a. Write the basic recommended steps for the design of a clocked synchronous sequential circuit. **(06 Marks)**

b. Compare synchronous and asynchronous counter. **(04 Marks)**

c. A sequential circuit has one input and one output. The state diagram is as shown in the Fig. Q8(c). Design the sequential circuit with J-K flip-flop. **(10 Marks)**

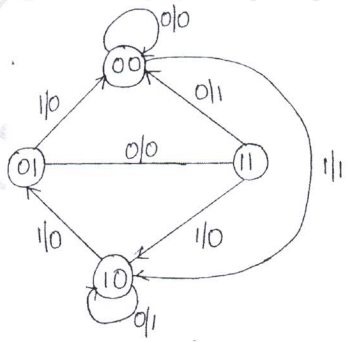

Fig. Q8(c)

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