Third Semester B.E. Degree Examination, June/July 2013
Logic Design

Time: 3 hrs. 　　　　　　　　　　　　　　　　　　　　Max. Marks:100

Note: *Answer FIVE full questions, selecting*
atleast TWO questions from each part.

PART – A

1　a. Simplify the following expression using Karnaugh map. Implement the simplified expression using the gates as indicated.

$f(a, b, c, d) = \Sigma m(0, 1, 2, 5, 6, 7, 8, 9, 10, 13, 14, 15)$ using only NAND gates

$f(A, B, C, D) = \pi m (0, 3, 4, 7, 8, 10, 12, 14) + \Sigma d(2, 6)$ using only NOR gates. **(12 Marks)**

　　b. Design a logic circuit that has 4 inputs, the output will only be high, when the majority of the inputs are high, use K map to simplify. **(08 Marks)**

2　a. Simplify using the Quine – Mcclusky minimization technique. Implement the simplified expression using basic gates

$V = f(a, b, c, d) = \Sigma(2, 3, 4, 5, 13, 15) + \Sigma d(8, 9, 10, 11)$. **(12 Marks)**

　　b. Simplify the logic function given below using variable entered mappings (VEM) technique
$f(A, B, C, D) = \Sigma m(0, 1, 3, 5, 6, 11, 13) + \Sigma d(4, 7)$. **(08 Marks)**

3　a. With the aid of block diagram, clearly distinguish between a decoder and encoder. **(04 Marks)**

　　b. Design a combinational logic circuit that will convert a straight BCD digit to an excess – 3 BCD digits
　　　i)　Construct the truth – table
　　　ii)　Simplify each output function using k map and write the reduced equations
　　　iii)　Draw the resulting logic diagram. **(12 Marks)**

　　c. Implement a full substractor using a decoder and NAND gates. **(04 Marks)**

4　a. Implement the following Boolean function using 4 : 1 multiplexer
$F(A, B, C) = \Sigma m (1, 3, 5, 6)$ **(04 Marks)**

　　b. Design a 2 bit comparator. **(08 Marks)**

　　c. What is a look ahead carry adder? Explain the circuit and operation of a 4 bit binary adder with look ahead carry. **(08 Marks)**

PART – B

5　a. Differentiate sequential logic circuit and combinational logic circuit. **(04 Marks)**

　　b. Explain with timings diagram the workings of a SR latch as a switch debouncer. **(08 Marks)**

　　c. Explain the workings of a master – slave JK flip flop with functional table and timings diagram. **(08 Marks)**

6　a. With the help of a diagram, explain the following with respect to shift register
　　　i)　Parallel in and serial out
　　　ii)　Ring counter and twisted rings counter. **(08 Marks)**

　　b. Explain the workings of 4 – bit asynchronous counter. **(04 Marks)**

　　c. Derive the characteristic equation of SR, JK, D and T flip – flops. **(08 Marks)**

7 a. With a suitable example, explain the mealy and Moore model of a sequential circuit.

(10 Marks)

   b. Design a synchronous counter using JK flip–flops to count the sequence 0, 1, 2, 4, 5, 6, 0, 1, 2 use static diagram and state table.

(10 Marks)

8 a. Design a clocked sequential circuit that operates according to the state diagram shown. Implement the circuit using D – flip – flop.
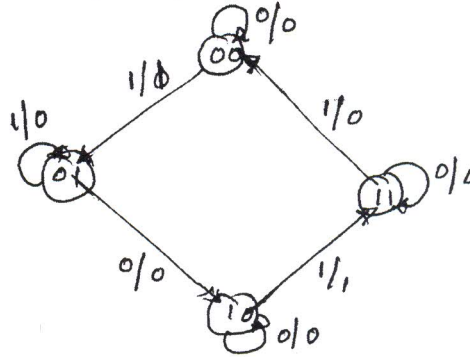
(12 Marks)

Fig. Q8(a)

   b. With a suitable, example and appropriate state diagram, explain how to recognize a particular sequence. EX 1011.

(08 Marks)

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