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10ES32

Third Semester B.E. Degree Examination, Dec.2016/Jan.2017
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the static and dynamic resistance of the diode. **(04 Marks)**

b. For the circuit shown in Fig. Q1 (b). Find I_D, V_1, V_2 and V_0. Assume silicon diode. **(08 Marks)**

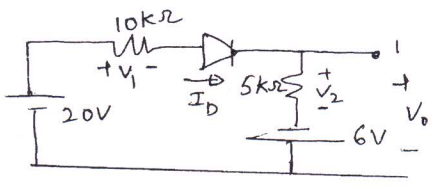

Fig. Q1 (b)

c. For the clipping circuit shown in Fig. Q1 (c). Draw the transfer characteristics and output voltage waveforms. Assume silicon diodes. **(08 Marks)**

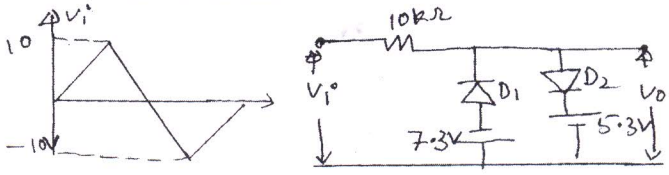

Fig. Q1 (c)

2 a. For a emitter bias circuit shown in Fig. Q2 (a). Find

i) Quiescent values of base and collector currents. ii) Quiescent values of V_{CE}.

iii) Voltage at base to ground and collector to ground. iv) Base to collector voltage.

Assume $V_{BE} = 0.7$ V, $\beta = 60$ **(10 Marks)**

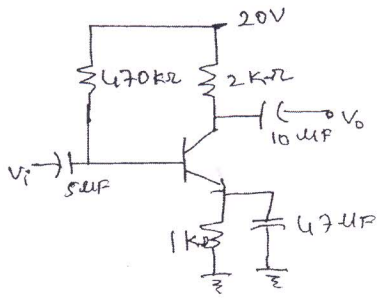

Fig. Q2 (a)

b. For the voltage divider bias configuration. Derive expression for I_C and V_{CE} and expression for collector current when it is in saturation. Comment on stability factor. **(10 Marks)**

3 a. Describe how transistor behaves as switch. Also describe transistor switching time. **(06 Marks)**

b. For common base npn transistor configuration with $I_E = 4$ mA, $\alpha = 0.98$ and ac signal of 2 mV applied between base and emitter terminals. Determine:

i) Input impedance ii) The voltage gain of load 0.56 KΩ is connected to output terminals.

iii) Output impedance. iv) Current gain. **(06 Marks)**

c. Explain common emitter fixed bias configuration. Derive expression for the input impedance, output impedance, voltage gain and current gain. **(08 Marks)**

4 a. Explain low frequency response of BJT amplifier. Derive the expression for lower cut-off frequency considering the effect of input coupling capacitor C_S. **(10 Marks)**

b. For the circuit shown in Fig. Q4 (b). Calculate (i) f_{Hi} and f_{Ho}. (ii) f_β and f_T

Take $C_{be} = 35$ P.F, $C_{bc} = 5$ P.F, $C_{ce} = 1$ PF, $C_{Wi} = 6$ PF, $C_{WO} = 10$ P.F, $\beta = 100$ and $V_0 = \infty$. **(10 Marks)**

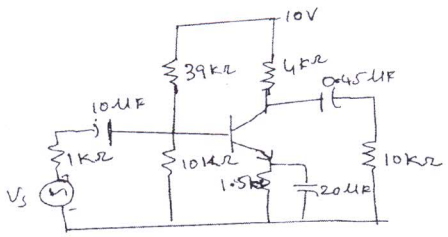

Fig. Q4 (b)

PART – B

5 a. Explain Darlington emitter follower. Draw the equivalent circuit. Derive expression for input impedance (Z_I), current gain (A_I), Voltage gain A_V and output impedance (Z_0). **(10 Marks)**

b. Determine the voltage gain, input and output impedance with voltage series feedback having $A = -100$, $R_i = 10$ KΩ, $R_0 = 20$ KΩ for feedback factor $\beta = -0.1$. **(06 Marks)**

c. Discuss the advantages of negative feedback. **(04 Marks)**

6 a. Describe FET amplifier with voltage series feedback. Derive the expression for gain. **(10 Marks)**

b. Explain the principles of class B amplifier operation. Derive expression for
(i) input dc power (ii) Output ac power (iii) η-efficiency
(iv) power dissipated by output transistor. **(10 Marks)**

7 a. Write the basic principle of oscillator. Also state the conditions for oscillation. **(04 Marks)**

b. Describe any one type of tunned oscillator with relevant diagram. Write expression for frequency of oscillations. **(08 Marks)**

c. RC phase shift oscillator $R_C = 5$ kΩ and $R = 3.3$ kΩ. Find the range of values of capacitor if it is required to vary frequency from 100 Hz to 20 kHz. **(08 Marks)**

8 a. Explain common gate JFET configuration with relevant circuit diagram. Draw equivalent circuit. Derive expression for Z_i, Z_0 and A_V. **(08 Marks)**

b. The self biased configuration of JFET has operating point defined by $V_{GSQ} = -2.6$ V and $I_{DQ} = 22.6$ mA and $I_{DSS} = 8$ mA and $V_P = -6$ V the value of $Y_{OS} = 20$ μS as shown in Fig.Q8 (b). Find (i) g_m (ii) r_d (iii) Z_i (iv) Z_0 **(06 Marks)**

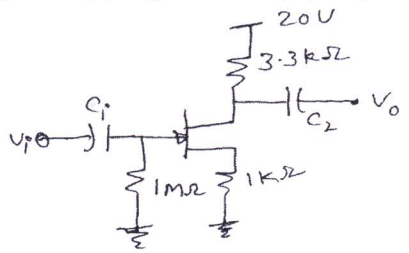

Fig. Q8 (b)

c. Differentiate depletion type MOSFET and enhancement type MOSFET. **(06 Marks)**

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