Third Semester B.E. Degree Examination, Dec.2015/Jan.2016 Analog Electronic Circuit

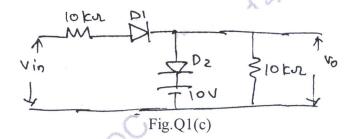
Time: 3 hrs.

Max. Marks:100

Note: Answer any FIVE full questions, selecting atleast TWO questions from each part.

PART - A

- a. With necessary equivalent circuit, explain the various diode equivalent circuits. (06 Marks)
 - b. What do you understand by reverse recovery time? Explain its importance in selection of a diode for an application. (06 Marks)
 - c. For the diode circuit shown in Fig. Q1(c) draw the transfer characteristics. The input is 40 sin ω t. Show clearly the steps of analysis. All diodes are ideal. (08 Marks)



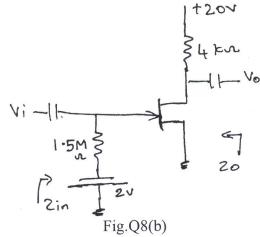
- 2 a. Discuss the effect of varying I_B and V_{CC} on the Q point. Explain your answer with relevant diagram. (06 Marks)
 - b. An emitter bias circuit has $R_C = 2 \text{ k}\Omega$, $R_E = 680 \Omega$, $V_E = 2.1 \text{ V}$, $V_{CE} = 7.3 \text{ V}$, $I_B = 20 \mu \text{A}$. Find V_{CC} , R_B and β .
 - c. A voltage divider biased circuit has $R_1=39~k\Omega$, $R_2=8.2~k\Omega$, $R_C=3.3~k\Omega$, $R_E=1~k\Omega$, $V_{CC}=18V$. The silicon transistor used has $\beta=120$. Find Q-point and stability factor.

(08 Marks)

- a. Derive an expression for voltage gain, input impedance and output impedance of an emitter follower amplifier using re-model. (06 Marks)
 - b. A voltage divider biased amplifier has $R_1 = 82 \text{ k}\Omega$, $R_2 = 22 \text{ k}\Omega$, $R_E = 1 \text{ k}\Omega$, $R_C = 2.2 \text{ k}\Omega$, $V_{CC} = 18 \text{ V}$. The silicon transistor has $\beta = 100$. Take $R_S = 1 \text{ k}\Omega$, $R_L = 5.6 \text{ k}\Omega$. Find voltage gain, input impedance, output impedance. (06 Marks)
 - c. A transistor in CE mode has $h_{ie} = 1100~\Omega$, $h_{fe} = 100$, $h_{re} = 2.5 \times 10^{-4}$, $h_{oe} = 25~\mu V$. Find voltage gain, input impedance and output impedance. Take $R_S = 1~k\Omega$, $R_L = 1~k\Omega$. Also find current gain.
- 4 a. Discuss with relevant equivalent circuit the method of determination of lower cutoff frequency for a voltage divider biased CE amplifier. (10 Marks)
 - b. A voltage divider biased CE amplifier has $R_S=1$ k Ω , $R_1=40$ k Ω , $R_2=10$ k Ω , $R_E=2$ k Ω , $R_C=2.2$ k Ω , $C_S=10$ μF , $C_C=1$ μF , $C_E=20$ μF , $\beta=100$, $V_{CC}=20$. The parasitic capacitance are $C_\pi(C_{be})=36$ pF, $C_\mu(C_{bc})=4$ pF, $C_{ce}=1$ pF, $C_{wi}=6$ pF, $C_{wo}=8$ pF. Determine higher cutoff frequency. (10 Marks)

PART - B

- 5 a. Obtain expression for voltage gain, input impedance and output impedance of a Darlington emitter follower. Draw necessary equivalent circuit. (08 Marks)
 - b. Mention the different configuration of feedback amplifiers and obtain expression for voltage gain with feedback for any one configuration. (06 Marks)
 - c. What are the advantages of cascading amplifiers? Obtain expression for overall voltage gain for an n stage cascaded amplifier. (06 Marks)
- 6 a. Prove that the maximum conversion efficiency of class A transformer coupled amplifier is 50%. (08 Marks)
 - b. With neat diagram, explain the methods of obtaining phase shift of input signal for class B operation. (06 Marks)
 - c. The harmonic distortion component in an power amplifier is $D_2 = 0.1$, $D_3 = 0.02$, $D_4 = 0.03$. The fundamental current amplitude is 4 A and it supplies a load of 8 Ω . Find total harmonic distortion, fundamental power and total power. (06 Marks)
- 7 a. What is Barkhansen criteria for sustained oscillation? Explain basic principle of operation of oscillators. (08 Marks)
 - b. With a neat circuit diagram, explain the working of Hartley oscillator. Write the equation for frequency of oscillations. (08 Marks)
 - c. A crystal has mounting capacitance of 10 pF. The inductance equivalent of mass is 1 mH, the frictional resistance = 1 k Ω and compliance = 1 pF. Find series and parallel resonant frequency. (04 Marks)
- 8 a. Obtain the expression for voltage gain, input impedance output impedance for a JFET common source amplifier with self bias configuration. (08 Marks)
 - b. For the FET amplifier in Fig. Q8(b), find voltage gain, input impedance and output impedance. The FET has I_{DSS} = 15 mA, V_p = -6V, Y_{OS} = 25 μ s. (08 Marks)



c. Mention the difference between BJT and FET.

(04 Marks)

* * * * *